

PART NUMBER	DESCRIPTION
PC1702802-4800	2A, 28 Vdc Solid-State Power Controller
PC1702807-4800	7A, 28 Vdc Solid-State Power Controller
PC17028152-4800	15A, 28 Vdc Solid-State Power Controller

These solid-state power controllers (SSPC) switch, monitor, report status and provide circuit protection for circuits from 2 to 15 amps within the voltage limits and conditions specified in MIL-STD-1275.



## FUNCTIONAL SPECIFICATIONS

### CONTROL INPUT

The device is controlled ON, OFF or RESET by a TTL level applied to the CONTROL pin (see Table 2).

### VBIAS INPUT

The VBIAS input provides power for the device. At power up (+28V present, VBIAS not present), the output of the SSPC shall be OFF regardless of the state of the CONTROL pin. When the VBIAS is present, the output of the SSPC shall follow the command of the input control. When VBIAS is removed, the device shall return to OFF condition regardless of the state of the CONTROL pin.

### LOAD STATUS OUTPUT

A TTL high at the LOAD ST pin indicates that the current flow is less than 15% of the rated device current. A TTL LOW indicates that the current flow is greater than 5% of the rated device current. For load current between 5% and 15% of the rated current, the LOAD status is undetermined and it may go either way.

### GATE STATUS OUTPUT

A TTL HIGH at the GATE ST pin (pin 4) indicates that the voltage on the gate of the power FET is HIGH. A TTL LOW indicates the voltage at the gate of the power FET is LOW.

### TRIP CHARACTERISTICS

The device shall interrupt the flow of load current when the current draw is equal to or is greater than 145% of the rated current. The device will NEVER trip when the current draw is equal to or less than 110% of the rated load. Between 110% and 145% of current draw rating, the device may or may not trip. The trip time is specified in Figure 4.

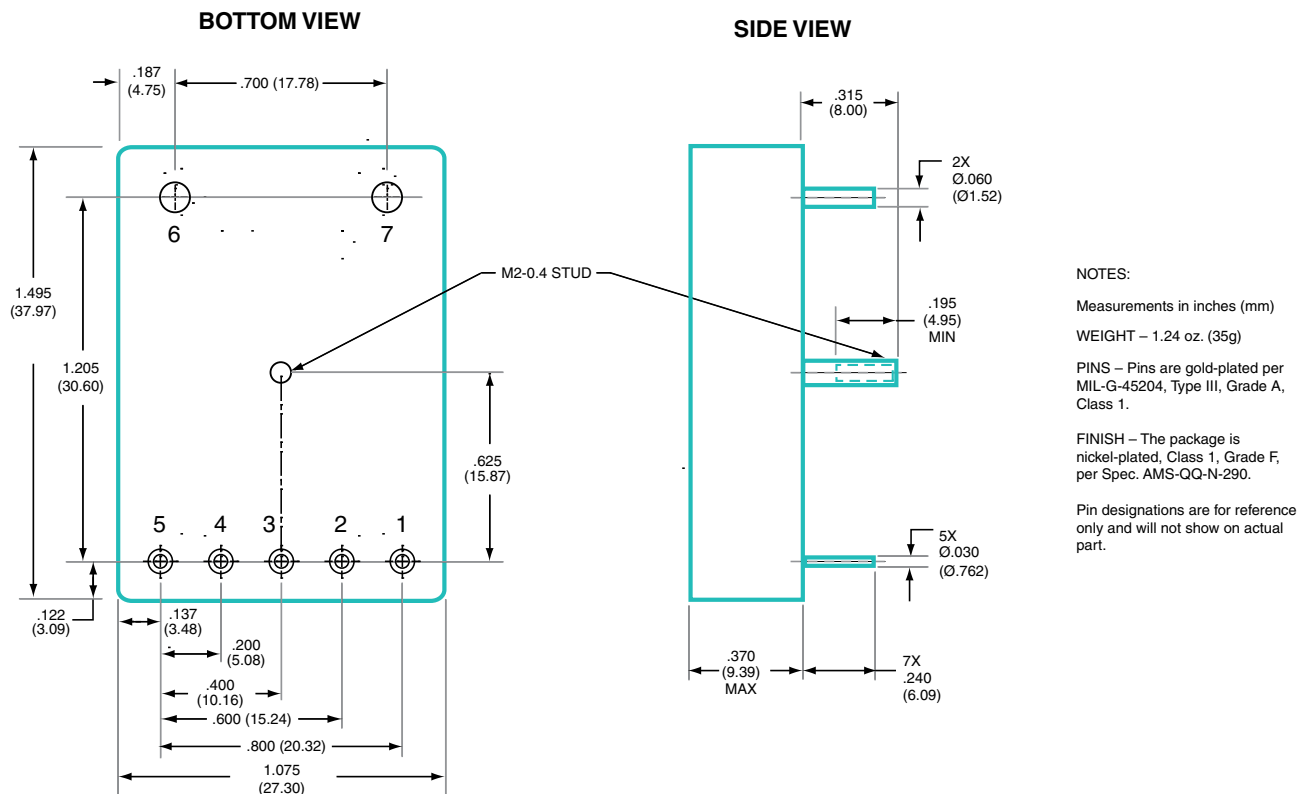
### POWER ON CONDITION

When the CONTROL input is LOW or OPEN, the device shall be OFF.

### STATUS CONDITIONS

The status and control of the device shall be monitored through the CONTROL, GATE ST and LOAD ST outputs as shown in Table 4.

FIGURE 1 – MECHANICAL OUTLINE



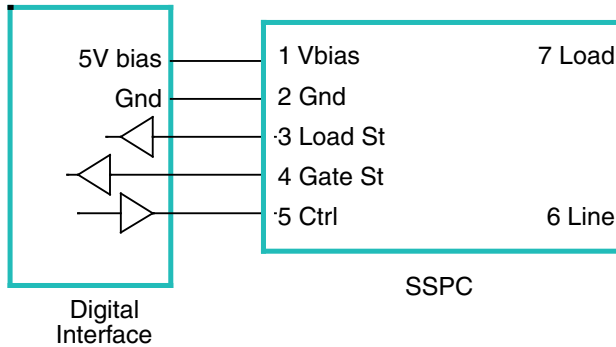
**TABLE 1 – TIMING REQUIREMENTS**

PARAMETER	SYMBOL	MAX	UNIT
CNTL to GATE ST delay	$t_0$	1000	usec
Turn on delay	$t_1$	200	usec
Load current rise time	$t_2$	1000	usec
Turn ON to LOAD ST delay	$t_3$	1000	usec
CNTL to GATE ST	$t_4$	1000	usec
Turn off delay	$t_5$	200	usec
Load current fall time	$t_6$	1000	usec
Turn off to load delay	$t_7$	1000	usec

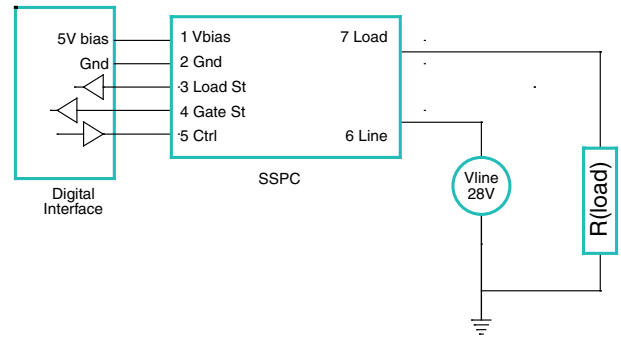
**NOTES:**

1. All timing measurements are at 10% and 90% into resistive load.
2. See Figure 2 for timing diagram.

**FIGURE 2 – TIMING DIAGRAM**



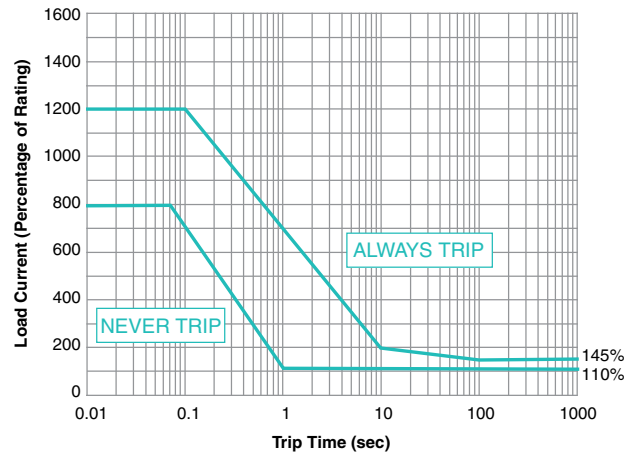
**FIGURE 3 – TYPICAL WIRING DIAGRAM**



**TABLE 3 – PIN OUT IDENTIFICATION**

PIN	NAME	I/O	DESCRIPTION
1	Bias	I	Control circuit input power
2	Gnd	–	Control circuit input ground, internally isolated from power ground
3	LOAD ST	O	Device load current status
4	GATE ST	O	Output power device drive gate status
5	Cntl	I	Device control input
6	Line	I	Line supply input
7	Load	O	Output to load

**FIGURE 4 – OVERLOAD TRIP TIME**



**TABLE 2 – DEVICE TURN ON AND TURN OFF**

Device Turn ON	TTL HIGH
Device Turn OFF	TTL LOW or OPEN
Device RESET (If Tripped)	TTL LOW for 50 mS. min. then HIGH

**TABLE 4 – STATUS AND CONTROL STATES**

STATE	CONTROL	GATE ST	LOAD ST	STATUS/CONDITION
1*	LOW	LOW	LOW	
2	LOW	LOW	HIGH	OFF
3*	LOW	HIGH	LOW	
4*	LOW	HIGH	HIGH	
5*	HIGH	LOW	LOW	
6	HIGH	LOW	HIGH	TRIPPED
7	HIGH	HIGH	LOW	ON, drawing > 5% rated load
8	HIGH	HIGH	HIGH	ON but drawing < 15% of rated load

\*State 1, 3, 4 and 5 are presently unassigned.

**TABLE 5 – ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	MAX	UNIT
<b>Input Specifications</b>				
BIAS Voltage	$V_{ihb}$	4.5	5.25	V
BIAS on Current Bias Voltage is 5.0V	$I_{ihb}$	–	30	mA
CONTROL Voltage High	$V_{ihc}$	2.4	5.5	V
CONTROL Voltage Low	$V_{ilc}$	–	0.8	V
CONTROL Current High Control Voltage at 5.0V	$I_{ihc}$	–	50	uA
CONTROL Current Low Control Voltage at 0.4V	$I_{ilc}$	–	-10	uA
<b>Output Specifications</b>				
LOAD Current	$I_l$	0	100	%RI
On State Voltage Drop	$V_{ld}$	–	200	mV
Line Voltage	$V_l$	0	32	V
GATE ST High Voltage	$V_{ohs}$	2.4	–	V
GATE ST High Current	$I_{ohs}$	–	50	uA
GATE ST Low Voltage	$V_{ols}$	–	0.8	V
GATE ST Low Current	$I_{ols}$	–	0.2	mA
Load Status Low	$I_{sonS}$	–	15	%RI
Load Status High	$I_{soff}$	5	–	%RI
LEAKAGE Current $V_{line} = 28 V$	$I_{ll}$	–	1	mA
TRIP Current	$I_{tr}$	110	145	%RI
Transients (VBias Input) PW=12.5 uS max Per MIL-PRF-28750	$V_{tb}$	+50		V
Spikes (28V Line) PW=10 uS max Per MIL-PRF-28750	$V_s$	-600	+600	V
Line Transient Voltage	$V_{is}$		50	V
<b>Isolation (Input-to-Output, All Pins-to-Case)</b>				
Dielectric Withstanding Voltage	$V_{dw}$		500	Vrms
Insulation Resistance	$R_{ins}$	100		Mohm

Note: %R<sub>l</sub> = % of rated device current

**TABLE 6 – QUALITY ASSURANCE PROVISIONS**

TEST	METHOD MIL-STD-883	CONDITION	REQUIREMENT
Internal Visual	2017		100%
Fine and Gross Leak	1014	A2	100%
Stabilization Bake	1008	150°C, 24 hrs	100%
Temperature Cycle	1010	B	100%
Constant Acceleration	2001	3000g, Y1 axis only	100%
Burn In*	1015	No load @ MOT, 72 hrs	100%
Final Electrical		Ambient	100%
Final Electrical @ Temp		Max. & min. operating temps	100%
External Visual	2009		100%

\*Open case burn-in allowed  
MOT = maximum operating temperature

**TABLE 7 – ENVIRONMENTAL SPECIFICATION**

PARAMETER	MIN	MAX	UNIT
Operating Temperature	-55	+100	°C
Storage Temperature	-55	+125	°C
Shock		MIL-STD-883, Method 2002, condition B; 1500g, 0.5msec	
Vibration		MIL-STD-883, Method 2007, test condition A; 20g, 20–2000 Hz	
Altitude		80,000	ft